REMARKS

Claims 1, 6 and 9-12 are amended. No new subject matter is added. Claims 1-15 remain pending in the case. Reconsideration and allowance of the pending claims is requested in light of the following remarks.

In the Claims

The amendments to claim 1 are fully supported by the original application at, e.g., claim 6, FIG. 3, and page 6, lines 29-31.

The amendments to claim 6 are fully supported by the original application at, e.g., claim 1, FIG. 4, and page 6, lines 29-31.

The amendments to claim 9 are fully supported by the original application at, e.g., claims 1 and 6, FIG. 4, and page 6, lines 29-31.

Claims 10 and 11 are amended for consistency with claim 9. The amendments to these claims are supported by the original application at, e.g., claims 10 and 11.

The amendments to claim 12 are fully supported by the original application at, e.g., claims 1 and 6, FIG. 4, and page 6, lines 29-31.

Drawings

The drawings are objected to under 37 CFR 1.83(a). Claim 1 is amended to overcome the objection the drawings. It was recognized that FIG. 3 illustrates two internal voltage generating circuits 20 and 30 arranged on both sides of the memory array 10.

Claim Rejections – 35 U.S.C. § 112

The amendment to claim 1 overcomes this rejection.

Claim Rejections – 35 U.S.C. § 103

Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,385,115 to Nakai ("Nakai") in view of U.S. Patent No. 6,314,035 to Kitade, et al. ("Kitade"). The applicant disagrees.

Nakai FIG. 2 illustrates an active sense amplifier power supply control circuit 1 that is illustrative of both of the active sense amplifier power supply control circuits 1a, 1b that are shown in FIG. 1 (column 9, lines 47-53). The active sense amplifier power supply control circuit 1 compares a reference voltage Vref1 with a control voltage Vint (FIG. 2; column 9, lines 55-57). Depending on the difference between the reference voltage Vref1 and the

control voltage Vint, the output of the comparator 1aa is either at a high (H) level or a low (L) level, which determines whether the current drive transistor 1ac is off or on (FIG. 2; column 10, lines 15-30). Therefore, the active sense amplifier power supply control circuit 1 maintains the control voltage Vint at the same level as the reference voltage Vref (FIG. 2; column 10, lines 31-33).

Nakai FIG. 4 illustrates a power supply driver 3 that is illustrative of the power supply drivers 3a0 – 3an+1, 3b0 – 3bn+1 shown in FIG. 1 (column 11, lines 31-35). As shown in FIG. 4, the N-channel MOS transistor 5c receives the control voltage Vint at its gate (column 11, lines 46-49).

Claim 1 recites first and second internal voltage generating circuits configured to compare a reference voltage to an internal voltage and to generate a comparing signal, where the comparing voltage is different from the internal voltage.

In the office action at page 4, lines 1-2, Nakai's FIG. 2 was interpreted such that the alleged comparing signal is the same as the alleged internal voltage Vint. Thus, Nakai fails to teach first and second internal voltage generating circuits that are configured to compare a reference voltage to an internal voltage and to generate a comparing signal, where the comparing signal is different from the internal voltage.

Kitade is not alleged to teach this feature of claim 1, nor does it teach this feature.

For the above reason, the combination of Nakai and Kitade fails to establish *prima facie* obviousness for claim 1 because it does not teach or suggest all the features recited in the claim. MPEP 2143.03.

Claims 2-5 are also allowable over the combination of Nakai and Kitade at least because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Claim 6 recites that the first and second active internal voltage generating circuits are configured to output a comparison signal that is generated by a comparator, that the comparator configured to generate the comparison signal based upon the difference between a reference voltage and an internal voltage, and that the first and second drivers are configured to supply the internal voltage to the internal voltage generating line in response to the comparison signal.

Contrary to the features recited in claim 6, it is apparent that Nakai's drivers 3 (FIG. 4) are not responsive to the comparison signal that is generated by the comparator 1aa of Nakai's active sense amplifier power supply control circuit 1 (FIG. 2).

Kitade is not alleged to teach this feature of claim 6, nor does it do so.

For the above reason, the combination of Nakai and Kitade fails to establish *prima facie* obviousness for claim 6 because it does not teach or suggest all the features recited in the claim. MPEP 2143.03.

Claims 7 and 8 are also allowable over the combination of Nakai and Kitade at least because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Claim 9 recites that the first and second active internal voltage generators include first and second comparators, respectively. Claim 9 further recites that outputs of the first and second comparators are coupled to inputs of the first and second drivers, respectively.

Contrary to the features recited in claim 9, the inputs of Nakai's drivers 3 (FIG. 4) are not coupled to the outputs of the first and second comparators 1aa (FIG. 2).

Kitade is not alleged to teach this feature of claim 9, nor does it do so.

For the above reason, the combination of Nakai and Kitade fails to establish *prima facie* obviousness for claim 9 because it does not teach or suggest all the features recited in the claim. MPEP 2143.03.

Claims 10 and 11 are also allowable over the combination of Nakai and Kitade at least because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Claim 12 recites directly coupling an output of a first comparator in a first active internal voltage generating circuit to an input of a first driver, and directly coupling an output of a second comparator in a second internal voltage generating circuit to an input of a second driver.

Contrary to the features recited in claim 12, the outputs of Nakai's first and second comparators 1aa (FIG. 2) are not directly coupled to the inputs of Nakai's drivers 3 (FIG. 4).

Kitade is not alleged to teach this feature of claim 12, nor does it do so.

For the above reason, the combination of Nakai and Kitade fails to establish *prima facie* obviousness for claim 12 because it does not teach or suggest all the features recited in the claim. MPEP 2143.03.

Claims 13-15 are also allowable over the combination of Nakai and Kitade at least because any claim that depends from a nonobvious independent claim is also nonobvious. MPEP 2143.03.

Conclusion

For the above reasons, reconsideration and allowance of the pending claims is requested. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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I hereby certify that this correspondence is being transmitted to the U.S. Patent and Trademark Office via facsimile number (571) 273-8300 on February 7, 2006.

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